REMARKS

In response to the above identified Office Action, Applicants respectfully request reconsideration in view of the following remarks. Applicants do not add, cancel, or amend any claims. Accordingly, claims 1-23 are pending.

I. Claims Rejected Under 35 U.S.C. § 102

Claims 1, 7 and 13 stand rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,647,464 issued to Reidlinger, et al (hereinafter "Reidlinger"). Applicants respectfully disagree for the following reasons.

In regard to claims 1, 7, and 13, these claims include the elements of "splitting a cache operation into two or more phases and two or more clock domains." The Examiner cites Fig. 2 of Reidlinger as teaching the claimed two or more phases and the two or more clock domains. However, the Applicants have reviewed Fig. 2 and Reidlinger in general and have been unable to discern any part therein that teaches the claimed two or more clock domains.

In the Final Office Action at page 8, the Examiner indicates that the pipeline operations in Fig. 2 of Reidlinger teach high and low clock phases and clock domains 0-5. However, the alleged 0-5 clock domains are, in fact, six **clock cycles**, in each of which an individual pipeline stage executes (col. 5, lines 60-62). While the Examiner is entitled to give a claim term its broadest interpretation, an interpretation that eviscerates the meaning commonly understood in the art is not reasonable. A clock domain, as commonly known in the art, is a part of a design driven by either a single clock or multiple clocks that have constant relationships (see, e.g., *Clock Domain Crossing*, a technical paper by Cadence Design System, Inc., 2004, page 1.) Different clock domains are a part of a design driven by clocks having variable time and phase

relationships (*Id.*). Fig. 2 of Reidlinger and the relevant portions of the disclosure (cols. 6-8) describe pipeline operations that occur in each clock cycle of **a single clock**. The operations in each clock cycle are synchronized such that the way select data (the result of the upper parallel path in Fig. 2) is received at the data array (the lower parallel path) by the end of the first phase of the LOW pipe stage (col. 8, lines 50-55). Reidlinger does not mention that the operations in the pipeline are clocked by different clocks of different clock domains that have variable time and phase relationships. Thus, Reidlinger discloses use of a single clock domain and not multiple clock domains as recited in claims 1, 7 and 13. Thus, Reidlinger does not teach each of the elements of these claims. Accordingly, reconsideration and withdrawal of the anticipation rejection of these claims are requested.

II. Claims Rejected Under 35 U.S.C. § 103

A. Claims 2-6, 8-10 and 14-18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Reidlinger in view of U.S. Patent No. 6,732,236 issued to Favor, et al. (hereinafter "Favor"). These claims depend from independent claims 1, 7 and 13 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to independent claims 1, 7 and 13, Reidlinger does not teach or suggest each of the elements of these claims. Favor does not cure the defects of Reidlinger. Specifically, Favor does not teach or suggest the use of multiple clock domains for a cache operation. Thus, Reidlinger in view of Favor does not teach or suggest each of the elements of these claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

B. Claims 11, 12 and 19-23 stand rejected under 35 U.S.C. § 103 as being unpatentable over Reidlinger in view of Favor and in further view of "Intel 865PE/865P Chipset Datasheet," hereinafter "Datasheet."

Claims 11 and 12 depend from independent claim 7 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to independent claim 7 Reidlinger and Favor do not teach or suggest each of the elements of this claim. Further, the Examiner has not relied upon Datasheet to cure these defects of Reidlinger and Favor. Specifically, the Examiner has not relied upon Datasheet to disclose the use of multiple clock domains. Thus, the Examiner has not established a *prima facie* case of obviousness for claims 11 and 12. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

In regard to claim 19-23 these claims include elements similar to those mentioned above in regard to independent claims 1, 7 and 13. Specifically, the use of multiple clock domains for a single cache operation is not disclosed in any of the cited references. Thus, for the reason mentioned above in regard to independent claim 1, 7 and 13, Reidlinger, Favor and Datasheet do not teach or suggest each of the elements of these claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 19-23 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-23, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

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Dated: August 7, 2006

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I hereby certify that this correspondence is being transmitted via facsimile on the date shown below to the United States Patent and Trademark Office.

Amber D. Saunders 8/7/06

Amber D. Saunders Date

TECHNICAL PAPER

cadence

CLOCK DOMAIN CROSSING

CLOSING THE LOOP ON CLOCK DOMAIN FUNCTIONAL IMPLEMENTATION PROBLEMS

1 OVERVIEW

Shrinking device sizes and increasingly complex designs have created multimillion-transistor systems running with multiple asynchronous clocks with frequencies as high as multiple gigahertz. SoC systems have multiple interfaces, some using standards with very different clock frequencies. Several modern serial interfaces are inherently asynchronous from the rest of the chip. There is also a trend toward designing major sub-blocks of SoCs to run on independent clocks to ease the problem of clock skew across large chips.

Design methodologies have traditionally focused on partition-based implementation and verification. Often these partitions are based on clock domains. The cross-clock domain crossing (CDC) signals pose a unique and challenging issue for verification. Traditional functional simulation is inadequate to verify clock domain crossings. While static timing analysis (STA) is an integral part of the timing closure solution, little attention has been paid to addressing proper clock domain implementation and verification. Existing methods provide an ad hoc partial verification that is manual, time consuming, and error prone.

If the sources of potential errors are not addressed and verified early on, designs can end up with functional errors that are only detected late in the design cycle—or even worse, during post-silicon verification. The cost of fixing errors at this stage is enormous. We know of large system houses in which chips are "dead in the water" due to CDC problems.

Several errors could be caused by cross-CDC signals:

- **Structural issues (sCDC):** If the data input to a storage element changes too close to a clock edge, the element may go into a metastable state and the output cannot be reliably used. Asynchronous clock domain crossings are particularly prone to metastability failures. To address this issue, the circuit must be designed to "buy time" so the metastable signal can settle to a stable value, typically using synchronizers.

  After completing the synchronization, the structures beyond the synchronizers still matter. For example, the design must ensure that the synchronized signals do not converge. Reconvergence can create functional errors.

- **Functional errors (fCDC):** Designers must ensure that the stability and functionality on either side of the CDC circuit are handed over properly. Otherwise, there could be loss of signal values for signals passing between clock domains, with data instability in the receiving clock domain.

Only automatic formal verification techniques can ensure that multiclock designs are correct prior to tapeout. The CDC verification solution must address this verification challenge, while maximizing overall productivity and effectiveness. The CDC solution needs to cover clock domain analysis and structural and functional verification, addressing both register-transfer-level (RTL) and gate-level verification needs. Utilizing the Cadence® CDC solution enables development teams to reduce the overall verification effort and lessen the risk of costly re-spins due to asynchronous clock domain crossing errors.

2 CDC BASICS

The design issues and challenges of handling the signal crossing domains will be discussed later in this paper. First, let's look at some CDC basics.

2.1 CLOCK DOMAINS

A clock domain is defined as that part of the design driven by either a single clock or clocks that have constant phase relationships. A clock and its inverted clock or its derived divide-by-two clocks are considered a clock domain (synchronous). Conversely, domains that have clocks with variable phase and time relationships are considered different clock domains.

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